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SHEET 1 OF 1

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(Modified) PATENT AND TRADEMAR		EMARK OFFICE	251148US0 * CRADELLE **		10/809,704		
APPLICANT							
LIST OF	REFER	ENCES CITED BY APP	PLICANT	Yuko UCHIMARU, et al.			
				FILING DATE		GROUP	
				March 26, 2004			
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7) (AO	2002-317049	10/31/2002	JAPAN (with English Abstract)		ļ	X
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ms	International Technology Roadmap for Semiconductors 2002 Update, 2002 Update Tables, page 75, "TABLE 62A MPU INTERCONNECT TECHNOLOGY REQUIREMENTS—NEAR-TERM", 2002						
m	AX	S. SHINMIYAHARA, et al., Cu-Interconnect Technology, page 227, "LATEST DEVELOPMENT OF CU WIRING TECHNIQUES", (with partial English translation)					
" 0	AY						
	AZ				Add	ditional Ref	erences sheet(s) attached
Examiner	L	may 1		Date Considered 5/5/68			
*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							